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PATENT ABSTRACTS OF JAPAN

(11)Publication number : 05-121793
(43)Date of publication of application : 18.05.1993

(51)Int.Cl. H01L 43/08
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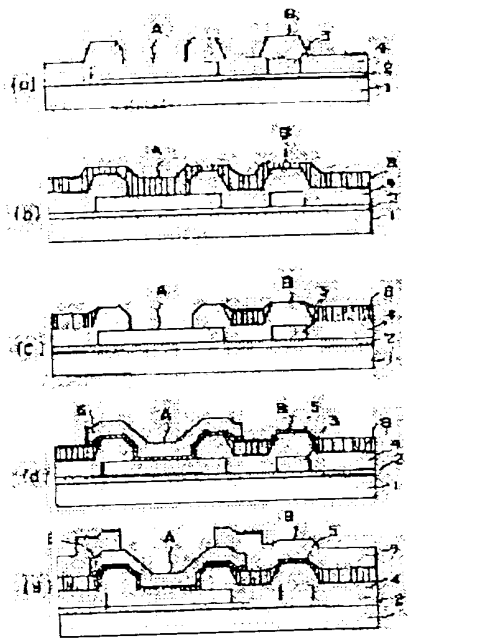
(21)Application number : 03-303796
(22)Date of filing : 24.10.1991

(71)Applicant : NEC CORP
(72)Inventor : YOSHIDA HISAO

(54) MANUFACTURE OF MAGNETORESISTIVE DEVICE

(57)Abstract:
PURPOSE: To make a magnetoresistive device tree from discontinuity and high in reliability to be formed on an IC section by a method wherein the sharply stepped surface of an IC is flattened.
CONSTITUTION: A sharp step located at an electrode A on an IC is flattened by a series of processes composed of a polyimide resin 8 applying operation, a dry-etching operation, a resist applying operation, and a patterning operation. By this setup, the sharp step located at the electrode A on an IC is flattened by the application of polyimide resin 8 and dry-etching, so that a magnetoresistive device high in reliability and free from disconnection can be formed on the IC even if a magnetoresistive device B is half as thick as a protective cover film formed on the IC.



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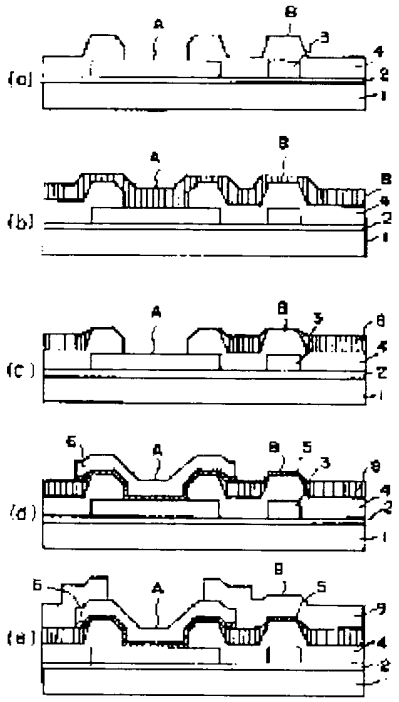

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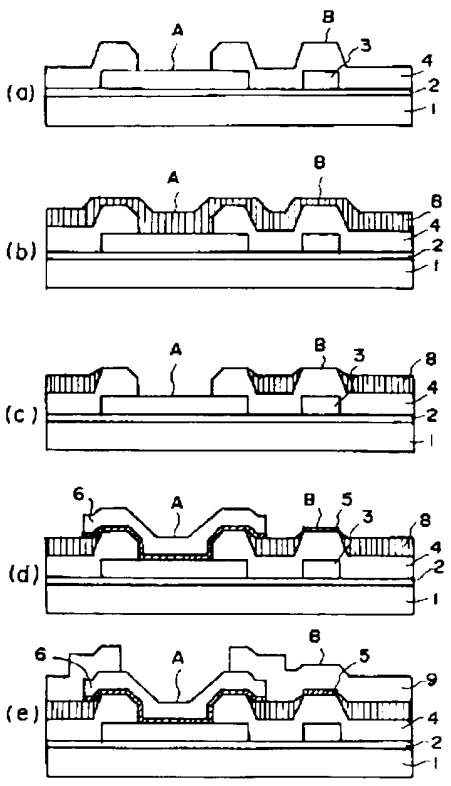

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] Especially this invention relates to the formation method of the resistance pattern which forms the magnetic-reluctance section on the IC section about the manufacture method of a magnetic-reluctance (MR:Magneto-resistive) element.
[0002]
[Description of the Prior Art] As shown in drawing 2 , the manufacture method of the conventional magnetic resistance element forms arbitrary patterns using a mask on the IC section in which the ground silicon oxide 2, aluminum 3, and the silicon nitride 4 were formed on the silicon substrate 1, after depositing the direct permalloy 5 and gold 6 continuously. After an appropriate time, a required pattern is formed for the protection silicon oxide 7, using the mask after spatter construction as a protective cover, and the polar zone A and the sensor section B are formed.
[0003]
[Problem(s) to be Solved by the Invention] Since the silicon nitride is thickly formed as a protective coat on the IC section especially when the IC section is formed upwards and it is going to form a magnetic resistance element by the manufacture method of the conventional magnetic resistance element (1-1.5 micrometers), the electrode section is steep.
[0004] Therefore, there was a trouble which will become easy to disconnect if the badness of the coverage of a portion with a steep level difference is expected and the vacuum evaporationo of the gold is not carried out more thickly [30 - 50% of silicon-nitride-film thick twists] when it is going to form the magnetic-reluctance section by carrying out the vacuum evaporationo of a permalloy and the gold on this.
[0005] The purpose of this invention is by carrying out flattening of the steep level difference of the polar zone of the IC section to form a magnetic resistance element with high reliability without an open circuit on the IC section.
[0006]
[Means for Solving the Problem] this invention is the manufacture method of the magnetic resistance element characterized by including the process which carries out flattening of the steep level difference on the IC section by a polyimide resin application and dry etching in the manufacture method of the magnetic resistance element which forms the magnetic-reluctance section on the IC section.
[0007] Furthermore, in this invention, the process from which portions other than the required polar zone other than the above-mentioned flattening process are protected by polyimide resin among the magnetic-reluctance sections on the IC section if needed is included.
[0008]
[Example] Next, the example of this invention is explained with reference to a drawing.
[0009] Drawing 1 (a) - (e) is the cross section of MR element shown in order of the process for explaining one example of this invention.
[0010] Drawing 1 (a) is the IC section which consists of a silicon substrate 1, the ground silicon oxide 2, aluminum 3, and a silicon nitride 4 first.
[0011] Next, polyimide resin (for flattening) 8 is put in on the IC section at the thermostat after 2 - 3-micrometer application, and it is made to harden enough, as shown in drawing 1 (b).
[0012] Next, a resist is exfoliated after performing plasma ablation and removing unnecessary polyimide resin (for flattening) 8, as shown in drawing 1 (c), and wet etching and plasma ablation fully removing the polyimide resin (for flattening) 8 of a resist application and the polar zone A after patterning using a mask further.
[0013] Next, a resist is exfoliated, after using a permalloy 5 and gold 6 by arbitrary thickness, using after vacuum evaporationo and a mask continuously and removing an unnecessary permalloy 5 and unnecessary gold 6 after a resist application and patterning, as shown in drawing 1 (d).
[0014] Next, as shown in drawing 1 (e), the mask after an application is used for thickness (2-3 micrometers) arbitrary on the whole surface for polyimide resin (for protection) 9, the resist after removal is exfoliated in the polyimide resin (for protection) 9 of a resist application and the polar zone A after patterning, the magnetic resistance element which contains polyimide resin (for protection) 9 after an appropriate time is put into a thermostat, and polyimide resin (for protection) 9 is fully stiffened.
[0015] As explained above, the manufacture method of the magnetic resistance element of this invention is also obtaining a magnetic resistance element with the high reliability which does not thicken golden thickness especially as a cure against an open circuit by carrying out flattening of the irregularity by applying polyimide resin (for flat), even if the film with a large level difference is formed.
[0016]
[Effect of the Invention] As explained above, in case this invention forms a magnetic resistance element on the IC section which has a steep level difference, it is effective in the ability to manufacture a magnetic resistance element with the high reliability which carries out flattening of the IC section top, and does not have an open circuit by performing plasma ablation for polyimide resin after an application and a baking bundle on the IC section beforehand.

[Translation done.]

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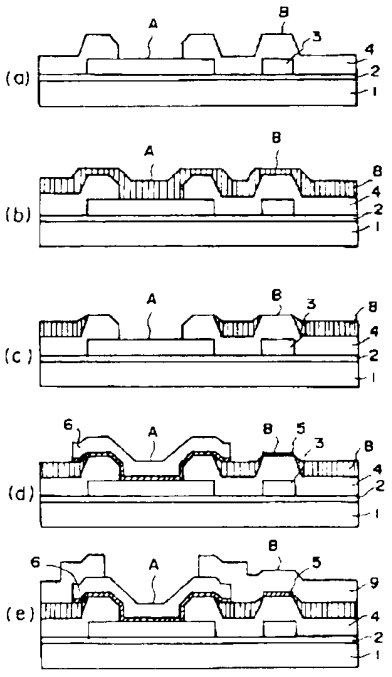
(54)【発明の名称】　磁気抵抗素子の製造方法

(57)【要約】

【目的】　ＩＣの急峻な段差を平坦化することによって断線のない信頼性の高い磁気抵抗素子をＩＣ部上に形成する。

【構成】　ＩＣ部上の電極部の急峻な段差を平坦化する為にポリイミド樹脂の塗布とドライエッチング及びレジスト塗布並びにパターニングによって構成する。

【効果】　ＩＣ部上の電極部の急峻な段差をポリイミド樹脂の塗布・ドライエッチングによって平坦化した為、ＩＣ部上の保護カバー膜厚の１／２の磁気抵抗素子部の膜厚でも断線のない信頼性の高い磁気抵抗素子をＩＣ部上に形成できる。



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【特許請求の範囲】

【請求項1】　ＩＣ部上に磁気抵抗部を形成する磁気抵抗素子の製造方法において、ＩＣ部上の急峻な段差をポリイミド樹脂塗布及びドライエッチングによって平坦化する工程を含むことを特徴とする磁気抵抗素子の製造方法。

【請求項2】　上記平坦化工程の他にＩＣ部上の磁気抵抗部のうち、必要な電極部以外の部分をポリイミド樹脂で保護する工程を含むことを特徴とする請求項1記載の磁気抵抗素子の製造方法。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は磁気抵抗（ＭＲ：Ｍａｇｎｅｔｏ－ｒｅｓｉｓｔｉｖｅ）素子の製造方法に関し、特にＩＣ部上に磁気抵抗部を形成する抵抗パターンの形成方法に関する。

【０００２】

【従来の技術】従来の磁気抵抗素子の製造方法は図２に示す様に、シリコン基板１上に下地酸化シリコン２、アルミニウム３、窒化シリコン４を形成したＩＣ部上に、直接パーマロイ５、金６を連続で蒸着した後、マスクを用いて任意のパターンを形成する。しかる後、保護カバーとして保護酸化シリコン７をスパッタ工事後マスクを用いて必要なパターンを形成して電極部Ａとセンサー部Ｂを形成している。

【０００３】

【発明が解決しようとする課題】従来の磁気抵抗素子の製造方法では、ＩＣ部を形成している上に磁気抵抗素子を形成しようとする場合には、特にＩＣ部上には保護膜として窒化シリコンが厚く形成されている為（１～１．５μｍ）、電極部が急峻となっている。

【０００４】従って、この上にパーマロイ、金を蒸着することによって磁気抵抗部を形成しようとする場合には段差の急峻な部分のカバレッジの悪さを見込んで、窒化シリコン膜厚より３０～５０％厚めに金を蒸着しないと断線しやすくなる問題点があった。

【０００５】本発明の目的はＩＣ部の電極部の急峻な段差を平坦化することにより断線のない信頼性の高い磁気抵抗素子をＩＣ部上に形成することにある。

【０００６】

【課題を解決するための手段】本発明はＩＣ部上に磁気抵抗部を形成する磁気抵抗素子の製造方法において、ＩＣ部上の急峻な段差をポリイミド樹脂塗布及びドライエッチングによって平坦化する工程を含むことを特徴とする磁気抵抗素子の製造方法である。

【０００７】更に本発明では、必要に応じて上記平坦化工程の他に、ＩＣ部上の磁気抵抗部のうち必要な電極部以外の部分をポリイミド樹脂で保護する工程を含む。

【０００８】

【実施例】次に本発明の実施例について図面を参照して

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説明する。

【０００９】図１（ａ）～（ｅ）は本発明の一実施例を説明する為の工程順に示すＭＲ素子の断面図である。

【００１０】まず図１（ａ）はシリコン基板１、下地酸化シリコン２、アルミニウム３、窒化シリコン４からなるＩＣ部である。

【００１１】次に図１（ｂ）に示す様にＩＣ部上にポリイミド樹脂（平坦化用）８を２～３μｍ塗布後恒温槽に入れて充分硬化させる。

【００１２】次に図１（ｃ）に示す様にプラズマ剥離を行なって不要なポリイミド樹脂（平坦化用）８を除去し、さらにマスクを用いてレジスト塗布・パターニング後電極部Ａのポリイミド樹脂（平坦化用）８をウェットエッチング及びプラズマ剥離によって充分に除去した後、レジストを剥離する。

【００１３】次に図１（ｄ）に示す様にパーマロイ５及び金６を任意の厚さで連続で蒸着後、マスクを用いてレジスト塗布・パターニング後不要なパーマロイ５及び金６を除去した後、レジストを剥離する。

【００１４】次に図１（ｅ）に示す様にポリイミド樹脂（保護用）９を全面に任意の厚さ（２～３μｍ）に塗布後マスクを用いてレジスト塗布・パターニング後電極部Ａのポリイミド樹脂（保護用）９を除去後レジストを剥離し、しかる後ポリイミド樹脂（保護用）９を含む磁気抵抗素子を恒温槽に入れ、ポリイミド樹脂（保護用）９を充分に硬化させる。

【００１５】以上説明した様に、本発明の磁気抵抗素子の製造方法は段差の大きい膜が形成されていても、ポリイミド樹脂（平坦用）を塗布することによって凹凸を平坦化することにより、断線対策として金の厚さを特に厚くすることのない信頼性の高い磁気抵抗素子を得ようとするのもである。

【００１６】

【発明の効果】以上説明した様に本発明は急峻な段差を有するＩＣ部上に磁気抵抗素子を形成する際、あらかじめＩＣ部上にポリイミド樹脂を塗布・焼きしめ後、プラズマ剥離を行なうことによってＩＣ部上を平坦化して断線のない信頼性の高い磁気抵抗素子を製造できる効果がある。

【図面の簡単な説明】

【図１】本発明方法の一実施例を説明するための工程順に示す時期抵抗素子の縦断面図

【図２】従来の磁気抵抗素子の製造方法を説明するための工程順に示す磁気抵抗素子の縦断面図

【符号の説明】

１　シリコン基板
２　下地酸化シリコン
３　アルミニウム
４　窒化シリコン
５　パーマロイ

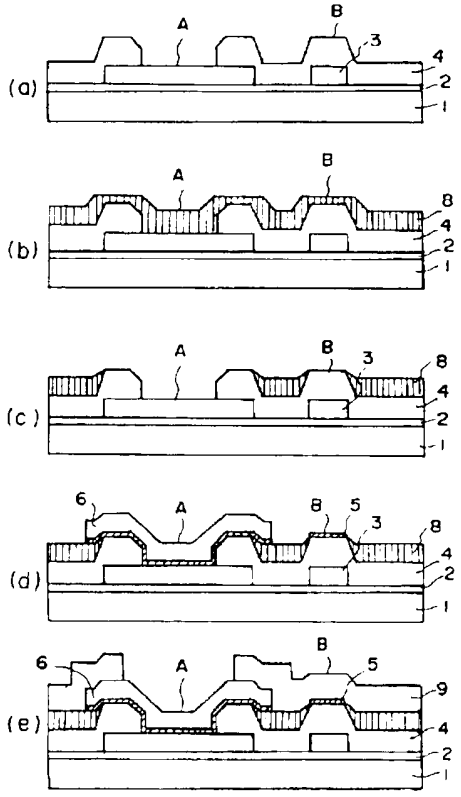
3

6　金
7　保護酸化シリコン
8　ポリイミド樹脂（平坦化用）

4

9　ポリイミド樹脂（保護用）
A　電極部
B　磁気抵抗部

【図1】



【図2】